June 9, 1999

Silicon Subsystem Report

May 1999

Subsystem Manager's Summary (M. Gilchriese)

Cost and Schedule Summary Status

Milestones corresponding to the baseline schedule are marked with a *. Additional milestones are included, and will be included, as needed to monitor progress

1.1.1 Pixel System

Costs are within allocated limits. There has been no major schedule change since last month, but the schedule for submission of the first rad-hard prototype IC, FE-D, remains the biggest concern. An Inner Detector Cooling Review was held at CERN on May 26-28. Preparations for this review, both calculations and measurements, took up a large part of the effort on mechanical systems. Presentations were made by Anderssen(2 of them), Bintinger and Miller. The outcome of the review was to confirm the use of evaporative cooling but to propose as a baseline fluid, mixtures that so far have had limited testing, particularly for pixel structures. We will have to understand the implications of this on our work plan and design in June, but the likely result is more work than planned in this area for the US. The fabrication of the first disk prototype is slightly behind the schedule given last month but the work is roughly 60% complete. Fabrication of the first panels for the prototype outer frame is on schedule as is the design and analysis of the structure. Work on integration and services is proceeding under the direction of Anderssen. There are a number of significant integration decisions that must be made in the next six months and he will present these to the pixel community at the Pixel Week in early June and a schedule for deciding. Work is proceeding well on the sensor design although some last minute minor, but useful, modifications have been suggested that impact the overall layout and testing. Delivery is still expected on schedule. There was a very successful test beam run in May-early June with many single-chip assemblies, include irradiated sensor 1b prototypes and a number of bare and flex modules. On-line analysis indicates that the changes made to reduce dead regions around the pixel implants were successful and the baseline processing for the 2nd sensor prototypes was decided. Progress continues to be made on the design and layout of FE-D and there will be a two-day internal review at Bonn in the first week of June. An LBNL engineer has been resident in Bonn for May to better coordinate the final integration and simulation. It has been agreed to pay Temic to accelerate the FE-D fabrication by about four weeks in the hope of having chips back in time to still test at CERN this year. We wont know until later in June if this is realistic or not. Analog test circuits fabricated in the Honeywell SoI process have been tested and look good. Tests are continuing at CERN where the engineer is now resident and irradiations are planned. The design of the flex hybrid v1.x is complete and will be fabricated at CERN and in a US company(R&D Circuits in New Jersey). Delivery from R&D is expected by mid-June and from CERN by early July. It is planned to assemble modules with these new hybrids in time for the next test beam cycle starting about July 21. Additional modules are under flip-chip assembly at IZM(Germany) and Alenia(Italy) in time for this run. Quality control of flip chip assembly and wafer thinning work is continuing in the US, as well as Europe with slow progress.

1.1.2 Silicon Strip System

Costs are increasing beyond the baseline cost estimate in a number of areas. Incentive payments must be made to both Temic and Honeywell to accelerate the fabrication of the ABCD and the ABC, respectively. With these payments, the ABCD will be delivered on the baseline schedule and the ABC will be 3.5 months later than the baseline schedule. However, testing of the first ABCD prototype indicated that backside metallization must be done to make these chips useful, and this cost was not anticipated in the baseline development estimate(although it was in production). The ABCD wafers must first be ground and then metallized and this will be done in both the US and in Europe(the US vendor has been used before for this purpose with good success but the European vendor is new and needs to be tried. The advantage of the European vendor is that Temic may assume the risk, although this remains to be proven). In addition, the cost in the US of test systems for the ABCD and ABC (and combined CAFE-ABC) has substantially exceeded the baseline estimate. This is primarily the result of understanding that these ICs must be tested (pre-rad) to clock speeds up to about twice the operational speed of 40MHz. After irradiation, the ICs slow down by about a factor of two and it is now believed necessary to test pre-rad to about twice 40 MHz to ensure having good chips post-rad. A dedicated system is under design at LBNL for this purpose but was not foreseen in the baseline estimate. In summary, a BCP will be submitted in early June to request funds to accelerate the IC fabs, to fund wafer grinding/metallization and to fund the incremental cost of materials and engineering labor for the high speed test system. Assuming acceptance of this BCP and, of course, working ICs, we expect to hold to our next major milestone, which is selection of the IC type by December 10, 1999. An IC review for this purpose has tentatively been scheduled for the first week in December at CERN.

On the good news front, testing of the CAFE-P has proceeded and so far looks good. Detailed tests of one chip have been done on a hybrid with the chip matched to an old CDP chip in place of the ABC. Channel-to-channel matching (pre-rad) was measured to be 1.7% compared to 4% on the previous CAFÉ-M. All functions are operational and within specifications before radiation at room temperature. Four chips were irradiated at the LBNL cyclotron. At month end, measurements of dynamic channel-to-channel matching had not been completed but measurements of DC offsets (which were determined to be the cause of the post-rad variation problem with the CAFÉ-M) were measured at 1% which should translate into a dynamic matching of 3-4% if no new problems were introduced by the re-design. The testing is going slowly because of lack of ABCs to use for dynamic testing. We are carefully using the few old CDP chips we have left from SSC days until the ABCs are ready. Dynamic tests of the irradiated chips will proceed in June along with temperature tests.

The design of the modified hybrids needed for the CAFE-P and ABC has been completed and orders are underway with two vendors with delivery expected in time to match the accelerated ABC schedule. These (and other) hybrids will also be used for ABCD testing. It has been generally agreed that both ABCD and CAFE-P/ABC systems will be tested extensively both at UCSC/LBNL and CERN to understand IC performance and a detailed program will be developed at the SCT week in early June.

Work has started to renovate ancient space at LBNL for SCT module assembly(and pixel module assembly) - to make two "clean" rooms for this purpose. This work is expected to be completed by the end of September and occupancy will begin in October.

1.1.3 ReadOut Driver System

The ROD program has undergone significant changes since Irvine has withdrawn from the Readout Driver project and so we present here a longer, and more detailed, summary than usual. Addressing manpower needs and schedule impact has been of high concern. Additional engineering manpower is available from LBNL but physicist (postdoc) labor is missing for code development and use for both the SCT and pixel groups. Currently available and planned manpower is shown below:

Existing Personnel

K. Dao(EE) (20%) will work on the decoder VHDL software. Khang developed the original code. He will be performing updates to the code and extensive documentation.

D. Fasching(Phys) (100%) will interface to the pixel community, represent the pixel interests in the DIG and provide simulation and testing software.

O. Hayes(Grad Student) (100%) will provide simulation and testing software.

R. Jared(EE) (50%) will provide overall coordination, and interfacing to the SCT community.

K. Marks(EE) (100%) will provide the lead engineering and design effort on the ROD.

M. Nagel(EE) (100%) will work on updating the gather and output multiplexer VHDL.

New Personnel to be added

New Post Doc to support the laboratory testing of the ROD.

New ENG (100%) to support the DSP software. A person has been identified and will be interviewed for the DSP software work. Jared is working on the arrangements.

This will result in 3.7 FTE EE and 3.0 FTE Physics personnel to work on the ROD and to continue pixel test beam support(which is understaffed at present). Irvine will continue to provide support for existing DSP modules in use in lab and beam tests. In addition fruitful discussions are under way with collaborators in England to support the test stands needed for the ROD. This should result in about 2 physics software people for this effort. In fact, John Hill is making up a plan for this test-stand/DAQ software/hardware.

The schedule has been reevaluated for the fabrication and testing of the prototype ROD. The result is a schedule with contingency that meets the February 2000 need for SCT module system testing.

SCT ROD C Code Simulation, (DF, OH) This effort is on going and expected to be completed by July 7. The simulation software has had much work and is nearing completion. This C code simulation covers event generation to the output of the ROD. It is used to study the system and check that the VHDL simulation and board measurements give the same results. Small effort will be used after completion to maintain the simulation code.

Pixel ROD C Code Simulation, (DF, OH) This effort is on going and expected to be completed by August 1. The simulation software has less work that the SCT software. Currently the Item that is controlling the completion is the definition of the operation of the pixel MCC chip. This C code simulation covers event generation to the output of the ROD. It is used to study the system and check that the VHDL simulation and board measurements give the same results. Small effort will be used after completion to maintain the simulation code.

ROD Architecture, (all) This task is on going and expected to be completed by July 15. The main thrust of this effort is to accurately define the role of the DSPs used for error recording, calibration and configuration.

Decoder VHDL Code, (KD) This task is starting on June 15 and completing on October 1. The code was originally written by Dao. Code will have minor modification and be well documented. The estimated duration is about 2 month. The scheduled duration of 3.5 months will have adequate contingency.

Gather VHDL Code, (MN) This task is starting on July 4 and completing on October 1. The code was originally written by Dao. Code will have minor modification and be well documented. The estimated duration is about 1 month. The schedule duration of 2.75 months will have adequate contingency.

Controller VHDL Code, (KM) This task is starting on August 1 and completing on November 1. This code has not been written before. Code functionality is being defined in the architectural effort. The estimated duration is 2 months. The schedule duration is 3 months

Output MUX VHDL Code, (MN) This task is starting on September 15 and completing on November 1. The code is relatively simple and expected to be completed in 2 weeks. The estimated duration is 1.5 months will have adequate contingency.

DSP Evaluation Setup, (DF and Student) This task is starting on July 1 and completing on August 15. Hardware orders are being place now so that the material will be on hand to start the development on time. The task is to make the DSP evaluation hardware work and write examples of test code.

DSP C Code, (DF, OH and New Post Doc.) This task is starting on August 1 and completing on December 1. This code is expected to provide the primitive functions needed for testing and evaluation of the ROD.

ROD Schematic Entry, (all) This task is ongoing and completing on November 1. The schematic entry is performed as soon as part selection and interconnectivity is known. The schematic is needed to perform the simulations.

ROD Board Fabrication and Loading, This task is staring November 1 and completing on December 1. Board fabrication and loading is a strait forward operation that will be performed in industry (1 week PC layout, 1 week PC fabrication (premium paid for short time turn around) and 2 weeks to load the boards.

ROD Data Primitive Software, (DF, OH and New post Doc.) This task is starting September 1 and completing December 1. Software is written to communicate date primitives over the VME back plane to the ROD. This layer of software is expected insulate the DAQ/testing software from the details of the processor/National Instruments VME interface to the ROD. The first instantiation of the software will probably be for the National Instruments VME interface. The processor interface will come at a later time.

ROD Testing Software, (DF, OH and New post Doc.) This task is starting on August 1 and completing on December 1. This is the layer of software that is written to use the data primitive software to communicate the user requests to the ROD. It also communicates to the user. Only the initial testing of the ROD is covered by this item. The main testing and evaluation software is expected to be written in England.

ROD Debugging and Testing, (all) This task is starting on December 1 and completing on February 1, 2000. Loading and debugging of the remaining prototype ROD will begin after this testing and acceptance by the user community.

Detailed Reports

1.1.1 Pixel System

1.1.1.1 Mechanics (E. Anderssen, D. Bintinger, M. Gilchriese)

Milestones	Baseline	Previous	Current	Status
*ID Eng. Review at CERN	20-Oct-98	20-Oct-98		Done
Select prototype ring concept	1-Nov-98	1-Feb-99		Done
Select materials for frame proto.	15-Mar-99	7-Apr-99		Done
Complete fab 1st prototype ring	1-Apr-99	15-May-99	30-Jun-99	Delay
Complete frame Phase I	1-Jul-99	1-Jul-99	1-Jul-99	OK
Complete fab 1st prototype disk	1-Jul-99	1-Jul-99	1-Jul-99	OK
*Select sector baseline concept	1-Sep-99	1-Sep-99	1-Sep-99	OK
*Module attachment CDR	1-Sep-99	1-Sep-99	1-Sep-99	OK
*Compl test of 5-disk prototypes	1-Sep-99	1-Sep-99	1-Sep-99	OK
Complete frame Phase II	1-Oct-99	1-Oct-99	1-Oct-99	OK
Complete frame Phase III	1-Feb-00	1-Feb-00	1-Feb-00	OK

LBNL

1.1.1.1.1 Design

Design studies for the overall pixel support frame continue by Hytec, Inc. FEA models were made of support frame panels to be compared to measurements. The overall support frame FEA model was refined to investigate stresses at the frame ends where connections are made to the SCT frame. These results were summarized in a presentation for the Pixel Week to be held in early June.

A substantial effort over the last month was made to understand cooling performance by calculation and measurement in preparation for the Inner Detector Cooling Review that took place on May 26-28 at CERN. Detailed calculations of the pressure drops in an evaporative C_4F_{10} system were made by Hytec using fluid models. The results indicate that exhaust piping sizes need to be increased. Calculations of pressure drops and temperatures for liquid C_6F_{14} were made using fluid properties from 3M. These calculations were compared with measurements(see below) and found to be in good agreement. Presentations of requirements, evaporative cooling and liquid cooling were made by Hytec or LBNL at the cooling review. The preliminary outcome of the cooling review was to continue evaporative cooling as the baseline system but with a mixture of fluids rather than pure C_4F_{10}. Although C_4F_{10} has the lowest operating pressure, its cooling capability is not sufficient for "worst case" electronics power dissipation as presently(and newly) estimated for both SCT and pixels. Higher pressure operation offered by a mixture of fluids eg. C_4F_{10} + C_3F_8 has greater cooling capability, but only limited testing has been done, and none so far on pixel prototype structures. Substantial work remains to understand a full evaporative system.

1.1.1.1.2 Development and Prototypes

ESLI, San Diego, has produced approximately 9 sectors of a planned 14 to be delivered for the prototype pixel sector disk. The glassy carbon tubes for the sectors are tested to 90 psi before sector assembly. The tubes rupture at 150 psi. The width of the triple-U shape of the tubes has been widened by approximately 2 mm to aid in collecting heat from the sector "overhang" modules.

Aluminum tube sector 4 has been tested for out-of-plane distortion, with and without dummy silicon modules, vs temperature change and coolant pressure variation. Distortions due to temperature change from 22C to -18C are at maximum 20 microns for a sector facing. The distortion are concentrated entirely at the extremities of the sector overhangs. This distortion is acceptable. Distortion vs coolant pressure is approximately 60 microns at the extremities of the overhangs for 3 bar (all pressures are above atmospheric) but increases to 150 microns at 4 bar with a residual distortion of 60 microns. The distortions at 4 bar are excessive. We have also tested out-of-plane distortion vs temperature and coolant pressure variation after coolant pressure cycling. The coolant pressure was cycled between 0 and 3 bar 20 times over a two day period. After pressure cycling out-of-plane distortions were approximately the same to those before pressure cycling. Also temperature performance was monitored with IR imaging before and after pressure cycling and was found to be identical The temperature response meets are requirements.

Progress on fabrication of the prototype disk ring has been slower than expected but tooling and cut facing parts have been sent to the assembly vendor. Assembly will occur in June.

Facing material prototypes have been made and tested for modulus and tensile strength. The measurements agree with expectations. Some panel material has been irradiated to 25 MRads and will be tested for modulus and tensile strength.

Tooling for fabrication of prototype panels for the outer frame was completed and sent to Allcomp. Prototype panels should be fabricated and ready for initial tests by mid-June.

A large number of measurements of the cooling performance using liquid C_6F_{14} were made and documented for the cooling review. Sectors and staves were tested. Pressure predictions were compared with measurements on long tubes. In general, there is good agreement between estimates of pressures and temperatures and calculations.

1.1.1.1.3 Disk Production

No activity.

1.1.1.2 Pixel Sensors (S. Seidel)

Milestones	Baseline	Previous	Current	Status
*Start market survey	2-Nov-98	1-Dec-98		Done
*2nd prototype PDR	1-Dec-98	1-Dec-98		Done
*Complete market survey	5-Mar-99	12-Feb-99		Done
*2nd prototype FDR	29-Mar-99	22-Feb-99		Done
*Compl. Test 1st prototypes	13-Apr-99	13-Apr-99		Done

*Compl. 2nd prototype design	27-Apr-99	27-Apr-99	1-May-99	Done
*Compl. Fab of 2nd prototypes	21-Sep-99	21-Sep-99	21-Sep-99	OK

1.1.1.2.1 Design

A small revision to the Second Prototype design was undertaken to address a suggestion made by K. Einsweiler.

1.1.1.2.2 Development and Prototypes

IV and breakdown voltage measurements of Prototype 1b and 1c sensors were completed. This study concerned approximately 140 tiles and single chip devices at New Mexico (and a comparable number of devices at Udine and Dortmund) and so provided good statistics for decisions about design options to be used in the Second Prototypes. Comparisons of the behavior of moderated p-spray devices before and after irradiation to high fluence showed these devices to operate as expected. Their “moderated” profile is expected to decrease capacitance between implants (and hence noise). On the basis of these measurements, the Second Prototypes will be fabricated entirely with the moderated p-spray design; half will use normal silicon and half will use oxygen-enriched silicon for its expected radiation hardness. Measurements of irradiated bumped sensors were also completed; the sensors can now be assembled into modules. Plots from the New Mexico measurements can be found at http://www.hep.phys.unm.edu/atlas_pixel/1_5_prototypes/. Hypertext on that page points to measurements at the other institutes. Pending one signature from Udine, the Second Prototype order is ready to be placed.

1.1.1.2.3 Production

First thoughts on the organization of the PRR were discussed. Igor Gorelov of New Mexico took responsibility for interfacing with the SCT Database Group to develop features of the database required for production pixel tracking.

1.1.1.3 Pixel Electronics (K. Einsweiler, R. Kass)

Milestones	Baseline	Previous	Current	Status
Compl. Design HSOI test die	16-Apr-98	1-Nov-98		Done
Compl. Fab HSOI test die	26-Aug-98	31-Mar-99		Done
Compl. Design DMILL test device	15-Dec-98	15-Dec-98		Done
Submit 2nd Honeywell SoI test die	15-Jan-99			Not known
1st design review of DMILL proto	25-Jan-99	23-Feb-99		Done
*FDR DMILL 1st prototype	25-Jan-99	15-Jun-99	15-Jun-99	Delay
*Compl. Design DMILL 1st	26-Feb-99	30-Jun-99	30-Jun-99	Delay

proto.				
1st design review of Honey. Proto	1-Jun-99	1-Oct-99	1-Oct-99	Delay
Compl. Eval. HSOI test die	1-Jul-99	1-Aug-99	1-Aug-99	Delay
*FDR Honeywell SoI 1st prototype	5-Mar-99	15-Nov-99	15-Nov-99	Delay
*Compl. Design Honey. SoI proto.	2-Apr-99	1-Dec-99	1-Dec-99	Delay
*Compl. Fab of DMILL 1st proto.	23-Jul-99	15-Oct-99	15-Oct-99	Delay
*Compl. Fab of Honey. SoI 1st proto	25-Aug-99	1-Mar-00	1-Mar-00	Delay
*Compl eval. DMILL prototype	9-Dec-99	1-Jun-00	1-Jun-00	Delay
*Compl eval HSOI prototype	15-Feb-00	1-Jun-00	1-Jun-00	Delay
*Review design approach	19-Jan-00	15-Jun-00	15-Jun-00	Delay
*Select rad-hard vendor	29-Jan-00	15-Jul-00	15-Jul-00	Delay

1.1.1.3.1 Design

LBNL

Our highest priority remains the DMILL front-end chip submission (FE-D). Our lead engineer has spent most of May in Bonn working together to integrate the complete chip and to work on the high level simulations.

The layout work for the blocks of the digital readout portion of the chip is now completed. A minor error (known for more than a year) has been fixed in the EOC, First simulations of the complete column pair and end of column have been performed, and minor buffer sizing adjustments have been made. We are concentrating on completing simulations of the digital readout using both SPICE (ELDO) and Verilog. In particular, creation and debugging of test vectors to properly exercise the circuitry is proceeding. So far, no additional problems have been uncovered. Most of the time remaining before submission will be spent on expanding the scope and coverage of these simulations in order to prove that the circuitry really does what we expect in all cases.

The Bonn group is now completing the floorplan of the full pixel array, including the integration of all the remaining analog blocks into the overall layout. The interconnection of all blocks is essentially complete. Block level verification is continuing. It appears that all necessary circuitry will fit into the required die area, but much optimization has been required, at considerable cost in time.

We are having a 2-day “internal review” meeting in Bonn on June 9-10 with all of the chip designers to go over the complete chip, and all of the verification and simulation work up to this time. Out of this we will produce a list of the remaining work before submission. Given our present status, I believe we could submit in early July, but it is difficult to be sure prior to this review meeting.

The complete reticle for the TEMIC engineering run has also been worked out. It will include two pixel array chips (FE-D). It will also include an MCC prototype from Genova containing many improvements towards a final version, but not yet representing a complete chip. There are also prototypes of opto-link chips (two versions of a receiver chip and one version of a driver chip). The opto-electronics designs are based on those of the SCT, but have been transferred from a commercial rad-soft bipolar process by Siegen and Ohio State University. A special process monitor bar is being developed by LBL to allow reliable extraction of SPICE models from the FE-D wafers so that we can cross-check our design performance against expectations. Finally, a rad-hard LVDS buffer is included which will allow us to make a complete rad-hard version of the single-chip support card that we use for testing single chips in the lab and testbeam. With this buffer, we have the capability to operate a single pixel chip (or electronics/sensor assembly) while it is being irradiated to LHC fluences.

Ohio State

The existing DORIC4 chip uses BICMOS technology with only NPN transistors to achieve a radiation tolerant design. We are developing a version of the DORIC4 chip using a radiation hard CMOS process (Honeywell SOI and/or DMILL). In consultation with the team that designed the DORIC4 we have put together a spice model of the chip which uses n-FETs and p-FETs.

We have simulated a complete version of the chip, excluding the LVDS drivers. This simulation includes a newly designed preamp and "delay control" amplifier (in the feedback loop). In the simulations both the 40 Mhz clock and the encoded data are successfully generated. A series of simulations to test the operational characteristics of the circuits have been performed by varying the bias voltages from 3 to 5.25 V and as well as varying various resistor values.

Future work includes adding drivers to the circuit and modeling the new circuit. Chuck Rush (OSU) has been in contact with Michal Ziolkowski (Siegen) concerning the design, simulation and layout of the chip. We are in the process of arranging a meeting in Siegen for late this month to prepare for a chip submission shortly thereafter.

1.1.1.3.2 Development and Prototypes

LBNL

We have spent three weeks in the H8 testbeam in May, performing a series of measurements on many different devices. The program included detailed measurements of the new prototype 1b sensor designs, measurements of MCM-D single chip devices that include some of the routing between sensors and electronics that might be used in the B-layer. The prototype 1b sensor designs, and in particular the new baseline "
look as though they will work well enough for ATLAS, although there is still some small charge collection losses near the special implant that is used for pre-biasing of the pixels

for testing purposes. For the MCM-D, no additional problems were observed, and detailed studies of the different routing schemes will continue to be pursued by the German groups.

We have re-measured the Lorentz angle in two irradiated assemblies from LBL and found that it is significantly reduced (to about 3 degrees) in sensors irradiated to 5 and 10 times 10^{14} fluence. Scaling to ATLAS magnetic fields, this means the Lorentz angle will decrease from about 12 degrees to 4 degrees during operation of the detector. This has some serious implications for the barrel layout design and performance, as the large tilt angle in the present design (about 17 degrees) will vastly over-compensate the Lorentz angle. The result will be significant charge sharing between pixels towards the end of the detector lifetime, thereby increasing the demands on the minimum threshold in the electronics. Some of the present testbeam data will allow us to understand this problem in more detail to verify how significant the reduction in efficiency could be towards the end of the sensor lifetime.

There will be an additional 2 weeks of testbeam in late July. We will also perform a final survey of prototype 1b sensor designs to provide complete studies of the implications of different optimizations on performance. In particular, there is a design with improved charge sharing, optimized for analog readout that will be tested.

The Honeywell SOI multi-project submission which we made in Nov. 98 has returned to LBL and undergone preliminary evaluation. No further work on testing this chip has been done at LBL, but we are working to set up a test program on the CERN IC tester to continue the testing in Geneva, where the chip designer is now resident. This should produce further results during June. We hope to irradiate several die in the 88” cyclotron at LBL before it shuts off for several months for maintenance.

1.1.1.3.3 Production

No activity.

1.1.1.4 Pixel Hybrids (R. Boyd, S. Timm)

Milestones	Baseline	Previous	Current	Status
* Compl. Assembly of 1st proto.	14-Jan-99	10-Nov-98		Done
* 1st prototype design review	18-Feb-99	18-Feb-99		Done
* Compl. Tests of 1.0 protos.	15-Apr-99	15-Mar-99		Done
* Select hybrid type	15-Apr-99	1- Mar-99		Done
Compl. Design of 1.x proto.	1 - Apr- 99	21-Apr-99		Done
Fabrication of 1.x compl		1-Aug-99	1-Aug-99	OK
Singulate 1.x proto compl		15-Aug-99	15-Aug-99	OK
Assembly of 1.x proto compl		1-Sep-99	1-Sep-99	OK
Prototype 1.x tests complete		15-Oct-99	15-Oct-99	OK
Module assy with 1.x compl		15-Sep-99	15-Sep-99	OK
Design of proto 2.0 begins		1-Sep-99	1-Sep-99	OK

1.1.1.4.1 Design

Oklahoma

Rusty Boyd participated in the May test beam at CERN during which the first data from a Flex Hybrid module was taken in the H8 beam line. He also served as a reviewer for the SCT sensor design review at CERN. A generic Flex Hybrid layout was submitted to five vendors for quotation, one of which responded positively. We are still working with them to develop a quotation. Refinements in the layout for R&D Circuits were submitted and delivery is expected the second week of June (Flex Hybrid v1.2). Because bare modules are still in short supply, we plan to reuse the module which could not be wire bonded in order to have a Flex Hybrid v1.x module ready in time for the July test beam. Because of their need to order special material, the CERN flex hybrids will not be available until mid-July (Flex Hybrid v1.1). A design meeting is being planned at LBNL for early July to set the design parameters for Flex Hybrid 2.0 and to develop better methods of assembly for modules. We also will discuss services routing for stave and sector modules, as this is planned to be included in the design.

1.1.1.4.2 Development

Simulations of the "H" buss architecture have shown that there is no structure in waveforms below 1 GHz, *i.e*., there are no reflections due to transmission line effects. Simulation models now include adhesive, cover layers and the silicon of the pixel sensor. The simulations are still performed using ideal SPICE sources as we are still awaiting delivery of SPICE models of the FE and MCC drivers and receivers. Simulations of the power lines are planned for June.

Albany

At Albany, progress continues in two fronts. We have obtained a quote on a probe card to read out the FE pads of the flex hybrid. We are now in possession of the coordinate drawing of the flex that we need to make this order. We have also initiated the process of making a jig to mount the flex hybrid properly on our probe station. We expect delivery in the next couple days of the PC which will run our VME setup to test modules.
measure one flex.

1.1.1.4.3 Production

No activity.

1.1.1.5 Pixel Modules (R. Boyd, K. Einsweiler, K. K. Gan, M. Gilchriese)

Milestones	Baseline	Previous	Current	Status
*Compl. 1st proto. Design	29-Oct-98	1-Mar-99		Done
*1st proto. Design review	18-Feb-99	18-Feb-99		Done
*Compl. Tests of 1st protos.	18-Mar-99	17-Sep-99	17-Sep-99	Delay
*Select module type		18-Mar-99	22-Feb-99	Done

*2nd proto. Design review 17-Sep-99 10-Sep-99 10-Sep-99 OK
1st prototypes will continue to be tested during the May and July test beam cycles.

1.1.1.5.1 Design/Engineering

LBNL

Discussions were held with IZM to attempt to understand differences between X-ray quality control done in the US and at IZM. It appears that IZM needs to be more careful and additional cross checks will be done in the future. IZM has failed so far with European vendors to thin bumped wafers to the desired thickness(150 microns). Since this was done successfully twice in the US, IZM will send a dummy wafer and a real wafer to LBNL for delivery to the local grinding vendor used before. A key issue for solder bump bonding is the reliability of thin (non-planar) die. Significant die warpage may result in regions of poor or no contact and this needs to be tested. LBNL will have the wafers ground and diced and return them to IZM. Also as a result of discussions with IZM, they will implement an additional mask step to protect wire bond pads from over etching during removal of the underbump metal. We have had problems with wire bonding to IZM-processed parts and this hopefully will eliminate this intermittent problem.

1.1.1.5.2 Development and Prototypes
LBNL
We have tested real modules with MCC chips, including one Flex module with MCC, in H8. This is the first time that complete modules have been in a beam. The additional DAQ software improvements to support this operation were provided by LBL and worked well. The results from the Flex module are still being analyzed, but are very promising. The efficiency and uniformity look very similar to the single chip devices studied up to this time. There were occasional readout problems which were not understood. These problems appear to arise from a weakness in the system design of the FE and MCC chips together, so that under some conditions, the MCC will stop transmitting data. Such problems have not been observed in the lab despite extensive testing, and are most likely provoked by some features of the noise environment in the testbeam. Over the coming weeks, further effort will be made to provoke failures in the lab as well, where all I/O nodes can be probed and studied using picoprobes, in order to isolate the causes for these problems.

There will be an additional 2 weeks of testbeam in late July, during which we should be able to test new Flex modules. These modules should include the more realistic Flex 1.x designs now being fabricated by CERN and RD Circuits. We will attempt to modify one of these modules so that we eliminate the present readout problems in FE-B chips with the upper 8 of 18 columns. This requires ion-beam surgery on each FE-B chip in the module, but fortunately the surgery is fairly simple, and there is some hope to get a reasonable yield for the modifications. This would allow us to read out every pixel on the module, rather than only 5/9 of the pixels as we do now, and is quite important for studying the performance of the module in the overlap region between chips.

Ohio State

The handling of the VCSELs has been greatly improved. After the failure of several prototype pick-up tools in releasing the tiny VCSEL (250 microns x 250 microns) due to the static charge on the tip, we now use a glass tube with 250-micron diameter tip for the pick up. An aquarium pump is used to produce the vacuum, controlled via a small hole on the tube which can be closed with a finger. This greatly improves the handling although it remains a difficult task. Another difficulty in the handling is that the VCSELs frequently fly off the 8” x 11” white paper used as a work area to help us locate the tiny black silicon chip. We now manipulate the VCSEL inside a small metal box to reduce the lost; metal is used so that the VCSEL will not stick to the wall due to static charge. The box is painted white to reduce the search time which is the main activity in the VCSEL manipulation.

The optical package has been greatly improved based on the experience gained from producing the first prototype. The base is now much simpler. The stopper on the base that maintains the 300 microns spacing between the fibre and the VCSEL/PIN is integrated into the cap instead. The three pockets for housing the VCSEL/PIN are now placed on the jig for chip mounting. We only have to machine precisely located pockets on several jigs instead of on thousands of bases. This should greatly improve the yield of the bases in the production. We use macor instead of aluminum silicate for this prototype, resulting in bases and caps with much sharper features. The caps also fit tightly with the bases, representing a significant improvement over the previous prototype. The next step is to mount the VCSELs and measure the coupled optical power.

1.1.1.5.3 Production

No activity.

1.1.2 Silicon Strips

1.1.2.1 IC Electronics (A.A. Grillo)

Milestones	Baseline	Previous	Current	Status
*Send out market survey	1-Sep-98	17-Aug-98	17-Aug-98	Done
*FDR for 2nd CAFÉ-M	15-Sep-98	11-Sep-98	11-Sep-98	Done
*Procurement in place for 2nd proto	9-Oct-98	13-Nov-98	13-Nov-98	Done
*FDR for 2nd ABC	23-Oct-98	26-Jan-99	26-Jan-99	Done
*Closing date for market survey	26-Oct-98	25-Sep-98	25-Sep-98	Done
*Submit 2nd CAFÉ-M	30-Oct-98	26-Jan-99	26-Jan-99	Done
*Issue call for tender	9-Nov-98	9-Nov-98	9-Nov-98	Done
*Submit 2nd ABC	16-Nov-98	1-May-99	1-May-99	Done
*FDR for 2nd ABCD	11-Dec-98	15-Dec-99	15-Dec-99	Done
*Closing date for tender	21-Dec-98	22-Jan-99	22-Jan-99	Done

*Submit 2nd ABCD	27-Jan-99	8-Apr-99	8-Apr-99	Done
*CERN finance comm. Approval	15-Mar-99	15-Mar-99	15-Mar-99	Done
*Frame contract in place	15-Apr-99	30-May-99	30-Jul-99	Delay
*Compl. Fab of 2nd CAFÉ-M	19-Apr-99	8-Apr-99	8-Apr-99	Done
*Compl. Fab of 2nd ABC	19-Apr-99	13-Sep-99	3-Aug-99	Delay
*Test systems complete	26-Apr-99	31-Jul-99	31-Jul-99	Delay
*1st ICs avail. For 2nd proto hybrid	18-May-99	30-Sep-99	30-Aug-99	Delay
*Compl. Fab of 2nd ABCD	30-Jun-99	23-Jul-99	26-Jun-99	OK
Compl. metallization 1st ABCD	------------	------------	15-Jul-99	OK

1.1.2.1.1 Design/Engineering

LBNL & UCSC

As reported last month, all three new IC designs are complete with the last (ABC) submitted on 1-May to Honeywell. See below for information on acceleration of fab processing. Unfortunately, two weeks after the ABC was submitted for fabrication another problem with the design was spotted by further simulations at LBNL using random data and sequencing patterns. The error manifests itself as an extra bit in the packet header or a missing bit in the packet trailer of the output data stream. The errors occur only in conditions when multiple triggers occur before the data processing from the first trigger has been completed and is also related to at least one of the ICs in the chain having no hit channels. It has been determined that the resulting data pattern can be detected and corrected by the Off-detector Electronics. Therefore, the bug will not prevent use of the ICs in full system tests; however, it reduces the robustness to single bit errors in the transmission system and must be fixed in a final system. The cause and fix are now being studied by designers at RAL and CERN. It appears that the source of the problem is a faulty circuit block (Read Out Controller) that is different in the ABC and the ABCD, although they should be the same (the problem does not appear in simulation of the ABCD). An older version of this block was included by RAL in the integration of the ABC and was not caught in the design review.

Progress continues on designs of test equipment for CAFÉ-P and ABC. All the hardware for the CAFÉ-P tester is in house except for the probe card. Two bids have been received for that and the order should be placed in early June with delivery in mid-July. For the ABC tester at LBNL; the PCBs have been designed; layout is in progress. Software development has started but represents a significant amount of work to be completed in the next two months.

1.1.2.1.2 Development and Prototypes

LBNL & UCSC

Testing of the CAFÉ-P has proceeded well this month. Detailed tests of one chip have been done on a hybrid with the chip matched to an old CDP chip in place of the ABC.

Channel-to-channel matching (pre-rad) was measured to be 1.7% compared to 4% on the previous CAFÉ-M. All functions are operational and within specifications before radiation at room temperature. Four chips were irradiated at the LBNL cyclotron. At month end, measurements of dynamic channel-to-channel matching had not been completed but measurements of DC offsets (which were determined to be the cause of the post-rad variation problem with the CAFÉ-M) were measured at 1% which should translate into a dynamic matching of 3-4% if no new problems were introduced by the re-design. The testing is going slowly because of lack of ABCs to use for dynamic testing. We are carefully using the few old CDP chips we have left from SSC days until the ABCs are ready. Dynamic tests of the irradiated chips will proceed in June along with temperature tests.

Incentive payments have been made to Temic and Honeywell to accelerate the fabrication of the ABCD and the ABC. The ABCD is due out from Temic on 26-June. However, this will be without backside metalization which was determined on the previous lot to be essential for good performance. Temic has identified a third-party to perform the metalization but as yet will not guarantee wafer quality after the metal is deposited. Therefore, we will probe the wafers first and then have the metal deposited and then re-probe before cutting the wafers for mounting ICs on hybrids. This will add approximate 2-3 weeks onto the schedule. Honeywell is targeting wafer delivery for 2-August. Efforts are being put into place at CERN, RAL, LBNL and UCSC to hand carry wafers between sites for wafer probe, saw, etc. to have chips available ASAP and possibly get a module with each type of chip into the CERN test beam at the end of September.

1.1.2.1.3 Production

Final negotiations between CERN and the two IC vendors, Temic and Honeywell, have not yet been completed and so the Frame Contract is not yet in place. A meeting with Temic is schedule for 7-June to finalize terms and conditions. A similar meeting with Honeywell is planned but not yet scheduled. At the moment, the lack of the Frame Contract has no impact on our schedule.

1.1.2.2 Silicon Strip Hybrids (C. Haber)

Milestones	Baseline	Previous	Current	Status
Complete design of 1st prototype	17-Nov-97	17-Nov-97		Done
Complete fab of 1st prototype	2-Feb-98	23-Mar-98		Done
Preliminary design review	3-Aug-98	1-May-99	15-Sep-99	Delay
*Compl. 2nd proto subs. design	29-Oct-98	15-May-99	15-Jun-99	Delay
*Compl. 2nd proto cable design	29-Oct-98	15-May-99	15-Jun-99	Delay
*Compl. 2nd proto fanout design	29-Oct-98	15-May-99	15-Jun-99	Delay
*Compl fab of 2nd proto substrate	11-Mar-99	1-Aug-99	1-Aug-99	Delay

*Compl fab of 2nd proto cable	11-Mar-99	1-Aug-99	1-Aug-99	Delay
*Compl fab of 2nd proto fanout	11-Mar-99	1-Aug-99	1-Aug-99	Delay
*Compl procure of 2nd proto comps	11-Mar-99	1-Aug-99	1-Jul-99	Delay
*Compl. 2nd proto assembly	17-May-99	15-Aug-99	15-Aug-99	Delay
*1st 2nd proto hybrids available	14-Jun-99	1-Sep-99	15-Aug-99	Delay

LBNL
1.1.2.2.1 Design

A final design review was held of the ABC chip in March 1999. Last month we finally received a new layout of the ABC chip. The new coordinates were checked and new reference drawings of the chip for the hybrid layout work were produced. The hybrid CAD draftsperson was given a set of changes to make to the layout in order to make it compatible with the new ABC chip. The first version of the new hybrid layout for the ABC and CAFE-P chip was received from the designer this month. Design verification of the hybrid layout for the ABC and CAFE-P continued through this month. It is nearly done and will be complete in early June 1999.

1.1.2.2.2 Development and prototype fab

The substrates to be used in the fabrication of the new hybrids were laser machined to provide for a through hole connection to the back side shield. These substrates were received back from the laser shop.

All the purchase orders to cover the hybrid fabrication were placed.

1.1.2.2.3 Production

No activity.

1.1.2.3 Modules for Silicon Strips(C. Haber)

Milestones	Baseline	Previous	Current	Status
*Preliminary design review	3-Aug-98	1-Apr-99	T BD	Delay
Complete fabrication of 1st dummy modules	15-Aug-98	15-Aug-98		Done
Prototype tooling complete	1-Apr-99	1-Aug-99	1-Aug-99	Delay
*Compl. Design of proto assy/test	14-Jun-99	15-Nov-99	15-Nov-99	Delay
*Compl. Fab of tooling for proto	14-Jun-99	15-Nov-99	15-Nov-99	Delay

LBNL
1.1.2.3.1 Design of Assembly and Test

A new version of the assembly software from Manchester is available and we are still studying the documentation.

1.1.2.3.2 Development and prototypes

A tooling workshop was held at the Rutherford Lab in the UK the week of May 24, 1999.

The new calibration plate was submitted for fabrication and is due back in early June 1999. The consensus approach to the detector spacing was adopted.

Beryllia facings for use in the next set of modules for the diagnostic hybrid were ordered and received.

An attempt was made to machine some of the PG for the test of thermal performance but it was unsuccessful. We are pursuing some alternate approaches based upon suggestions received from Europe. Additional thermal filler has been ordered.

Design continued on a folding fixture for the hybrids.

The process of training a new technician on the assembly system continues. This individual is expected to be the lead technician on the module assembly during the construction phase. The plan is to build a thermal test hybrid. ABCD chips were loaded on a wrap-around pair of diagnostic hybrids and wirebonded. This will be the basis of the thermal module test.

1.1.2.3.3 Production

No activity.

1.1.3 ReadOut Drivers(A. Lankford,R. Jared)

Milestones	Baseline	Previous	Current	Status
*Select PreROD implementation	30-Oct-98	26-Mar-99		Done
*Requirements review	30-Nov-98	18-Nov-98		Done
*Compl. System design	28-Dec-98	TBD	TBD	TBD
*System design review	11-Jan-99	TBD	TBD	TBD
*Compl. PreROD design	29-Jan-99	TBD	TBD	TBD
*Compl. PreROD layout	15-Feb-99	TBD	TBD	TBD
*Compl. PreROD procure	1-Mar-99	TBD	TBD	TBD
*Compl. PreROD PCB fab	16-Mar-99	TBD	TBD	TBD
*Compl. PreROD 1st assemble	30-Mar-99	TBD	TBD	TBD
*Compl. Test stand requirements	14-Apr-99	14-Apr-99	TBD	TBD
*Compl. Test stand essential mod.	12-May-99	12-May-99	TBD	TBD
*Compl. Test stand impl. Model	10-Jun-99	10-Jun-99	TBD	TBD
*Compl. PreROD assembly	9-Jul-99	TBD	TBD	TBD

*PreRODs complete	20-Aug-99	TBD	TBD	TBD
*Test stand design review	21-Sep-99	21-Sep-99	21-Sep-99	OK
*Compl. Design of test stand	28-Sep-99	28-Sep-99	28-Sep-99	OK
*LVL2/ROB interfaces compl.	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD Common design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD strip design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK
*ROD pixel design PDR	1-Oct-99	1-Oct-99	1-Oct-99	OK

A revised schedule will be available for the July monthly report or after approval of a BCP submitted in July.

1.1.3.1.1 Strip Test Beam Support

DSP support for the existing DSPs will be provided by Irvine and will not be covered in this report.

1.1.3.1.2 Pixel Test Beam Support

Minor support effort was supplied in May. Finally, for PLL's, two modules developed minor problems during the recent testbeam period, and they have been returned to LBL for testing and repair. Several modules from the original January production remain to be completely debugged. It is clear that the support in this area from the ROD group needs to be significantly increased in order to deliver all of the modules and keep them working in outside institutions.

1.1.3.2.1 ROD Requirements

Initial contacts have been made with the user community to define and justify the following requirements.

1. Monitoring of the ROD data flow status (buffer occupancy, S-Link status, front-end status, etc) as recommended in the recent ROD review. John Hill that heads the ROD crate processor effort will assist in this effort
2. Dynamic throttling of individual links during data taking. This would be based on the measured number of events in the front-end modules.
3. Issue configuration commands during the periodic reset.
4. The number and speed of pixel lengths into a ROD. This question is governed by what capabilities can be designed into the module control chip.

1.1.3.2.2 ROD Essential Model

The essential model defines the essential functionality of the ROD and defines the interfaces of the ROD to other functional units. It is complete, except for refinements that are ongoing during the development of the implementation model. No refinements of the essential model were made during May

1.1.3.2.3 ROD Implementation Model

Much work has been performed to understand the best use of the DSPs. Initial findings find that the DSPs can be used for control during calibration (one DSP controlling configuration and commands to the front-end chip and others performing analysis of calibration data) and one DSP used to monitor errors and corrections. In all cases the main data path latency and bandwidth is not effected by the DSPs. The above configuration of the DSPs has been shown to be a good model. Many details such as messaging and contents are being understood. Changes such as changing the decoder input processing from serial data to parallel data are being prepared as the bases of the development of the VHDL code that will start in two weeks.

1.1.3.3.7 Preprototype ROD

The preprototype ROD is now defined as the prototype ROD. This change has been made to shorten the development cycle. Meetings in early June have been set with our United Kingdom collaborators to address interface issues and verify that their schedule and the US schedule are in agreements. The architectural issues being addressed under 1.1.3.2.3 above apply directly to the prototype ROD.

The pixels RODs are being added to the simulation. Currently the simulation is from event generation to the output of the decoder. This activity will take two months to complete.